IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	SALTERS
Application No.	:	10/525,662
Filed	:	02/25/2005
For	:	DEVICE WRITING TO A PLURALITY OF ROWS IN A MEMORY MATRIX SIMULTANEOUSLY

APPEAL BRIEF

On Appeal from Group Art Unit 2827

Date: 5/31/2008

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Michael Ure
(Name)

(Signature and Date)

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I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-10 are pending, all of which stand finally rejected and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a memory in which plural rows are written simultaneously. To simplify a driver arrangement, cell strength control circuit is provided that reduces a supply voltage applied to individual ones of the memory cells and hence to

reduce drive strengths required to write data into the individual ones of the memory cells, relative to a drive strength of the bit line circuits, in dependence upon a number of memory cells being simultaneously written, at least during simultaneous writing of data into the memory cells in a plurality of the rows.

The following analysis of independent claim 1 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
1. A device with a memory, the device comprising		
a matrix of static memory cells functionally arranged in rows and columns;	FIG. 1a, 1	Page 3, lines 8-17
bit line circuits, each for writing data to memory cells in a respective one of the columns;	FIG. 1a, 14a,b	Page 3, lines 8-17
a word line circuit constructed so that the word line circuit is capable of selecting memory cells in a plurality of the rows simultaneously to receive write data from the bit line driver circuits;	FIG. 1a, 18	Page 3, lines 8-17
cell strength control circuitry coupled to the cells and arranged to reduce a supply voltage applied to individual ones of the memory cells and hence to reduce drive strengths required to write data into the individual ones of the memory cells, relative to a drive strength of the bit line circuits, in dependence upon a number of memory cells being simultaneously written, at least during simultaneous writing of	FIG. 1a, 17; FIG. 4.	Page 4, line 31, to page 5, line 17; page 5, lines 25-33.

data into the memory cells in a plurality of the rows.		

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. under 35 USC 103, claims 1-10 are unpatentable over Ishida in view of Tomita and further in view of Haddad.

VII. ARGUMENT

I. Rejection of Claims 1-10 as Unpatentable Over Ishida in View of Tomita and Further in View of Haddad

The rejection recognizes that Ishida fails to disclose selecting a plurality of rows simultaneously but asserts that Tomita supplies this missing teaching. The rejection further recognizes that Tomita fails to disclose reducing drive strength in dependence upon a number cells simultaneously selected but asserts that Haddad supplies this missing teaching. For the following reasons, it would not have been obvious to combine the teachings of the references in the manner suggested.

Applicant submits that the interpretation urged by the Examiner is not a reasonable one.

Ishida teaches the use of an internal voltage decreasing circuit 11 to supply a predetermined precharge voltage (e.g., Vcc/2) separately to, on the input side, the memory array as a whole, and on the output side, to a selected bit line only. Size and drive strength of the internal voltage decreasing circuit 11 are therefore decreased. The voltage decreasing circuit 11, used to precharge the bit lines of a memory, *does not in any way affect the latching strength of the memory cells themselves.* (Compare Ishida, Fig. 9, showing memory cell 3a with Fig. 2 and 4 of the present specification. In the present specification, the power supply input 24 of the cells is connected to the output of the power supply reduction circuit as described in the paragraph bridging pages 4 and 5.)

Tomita describes an arrangement for burn-in (accelerated failure) testing of a memory in which many word lines are activated in parallel. A gating function (chip activation/deactivation function) is provided to prevent excessive current flow during

such burn-in testing wherein a large number of chips are arrayed on a burn-in board. Although not explicitly stated, presumably by activating a large number of word lines in parallel, the memory is rapidly "striped" with a data pattern suitable for test.

The combination of Ishida and Tomita has little bearing on the present invention apart from the fact that both relate in general to semiconductor memories.

Finally, Haddad relates to programming of a flash memory cell. A source bias voltage is applied to all cells. A gate control voltage is ramped from an initial lower voltage to a final higher voltage during the programming operation. Referring to Fig. 2 of Hammad, the supply voltages of the cell 204 are V_D and Vs. Because the voltage Vs is raised in relation to the voltage V_D, it may be argued that the supply voltage to the cells is reduced. However, such reduction is applied to all cells and is not performed "in dependence upon a number of memory cells being simultaneously written," as claimed.

Furthermore, because of the structure of flash memory cells (as compared to SRAM and DRAM cells, for example), the voltage V_D is applied *to the bitline itself* as seen in Fig. 2 of Haddad. Hence in Haddad, there can be no "reduction of a supply voltage applied to individual ones of the memory cells and hence to reduce drive strengths required to write data into the individual ones of the memory cells, *relative to a drive strength of the bit line circuits*," as claimed.

Thus it may be seen that the combination of references in no way teaches or suggests the invention of claim 1, including "cell strength control circuitry coupled to the cells and arranged to reduce a supply voltage applied to individual ones of the memory cells and hence to reduce drive strengths required to write data into the individual ones of the memory cells, relative to a drive strength of the bit line circuits, in dependence upon a

number of memory cells being simultaneously written, at least during simultaneous writing of data into the memory cells in a plurality of the rows," as claimed.

With regard to dependent claims 2-10, these claims depend from independent claim 1, which has been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claim.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: 5/31/2008

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A device with a memory, the device comprising

a matrix of static memory cells functionally arranged in rows and columns;

bit line circuits, each for writing data to memory cells in a respective one of the columns;

a word line circuit constructed so that the word line circuit is capable of selecting memory cells in a plurality of the rows simultaneously to receive write data from the bit line driver circuits;

cell strength control circuitry coupled to the cells and arranged to reduce a supply voltage applied to individual ones of the memory cells and hence to reduce drive strengths required to write data into the individual ones of the memory cells, relative to a drive strength of the bit line circuits, in dependence upon a number of memory cells being simultaneously written, at least during simultaneous writing of data into the memory cells in a plurality of the rows.

2. A device according to claim 1, wherein the cell strength control circuitry comprises a power supply reduction circuit coupled between a common power supply and an internal power supply line, the memory cells of at least one of the columns having power supply inputs coupled the internal power supply line, the power supply reduction circuit being arranged to provide a power supply voltage drop time-selectively at least during writing of data into the memory cells.

3. A device according to claim 2, wherein the power supply reduction circuit comprises a resistive element coupled between the common power supply and the internal power supply line.

4. A device according to claim 2, wherein the resistive element comprises a transistor, with a main current channel coupled between the common power supply and the internal power supply line.

5. A device according to claim 2, wherein the bit line circuit for the at least one of the columns comprises a bit-line driver circuit with a power supply input coupled to the internal power supply line.

6. (Previously presented) A device according to claim 5, wherein the bit-line driver circuit has a control input coupled to receive a control voltage derived from the common power supply line, substantially unaffected by said drop.

7. A device according to claim 1, wherein the cell strength control circuitry comprises a plurality of power supply reduction circuits, each coupled between a common power supply and a respective internal power supply line, the memory cells in respective ones of the columns each having power supply inputs coupled a respective one of the internal power supply lines, each power supply reduction circuit being arranged to provide a respective power supply voltage drop on the respective one of the internal power supply lines to which that power supply reduction circuit is coupled, selectively at least during

writing of data into the memory cells.

8. A device according to claim 7, wherein each power supply reduction circuit comprises a resistive element coupled between the common power supply and a respective one of the internal power supply lines.

9. A device according to claim 7, wherein the bit line circuit for each respective one of the columns comprises a respective bit-line driver circuit with a power supply input coupled to the internal power supply line of that respective one of the columns.

10. A device according to claim 9, wherein each bit-line driver circuit has a control input coupled to receive a control voltage derived from the common power supply line, substantially unaffected by said drop.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE